AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0016] with the following amended paragraph:

[0016] Fig. 3 is a block diagram showing one transceiver 130 that can be fabricated in integrated circuit 100 of Fig. 1. Transceiver 130 interfaces with an external device (not shown) through an output port 132 that supports differential output signals and an input port 134 that receives differential input signals. Transceiver 130 interfaces with programmable fabric 106 through a transmit data path 136, a receive data path 138, a plurality of clock signals (shown collectively as a signal line 140), a CRC (cyclic redundancy code) status signal 142, and a loss of synchronization signal 144. In one embodiment, the width of the data paths 136 and 138 can be independently configurably selected to be 1, 2 or 4 bytes. This allows engineering trade–offs in programmable fabric 106 between a wide data path with a low clock frequency versus a narrow data path with a high clock frequency. More detailed description of the configurable datapath can be found in a copending patent application entitled "Variable Data Width Operation In Multi-Gigabit Transceivers On A Programmable Logic Device," filed concurrently on March 1, 2002 by Cory et al., Patent Application Serial Number 10/090,286. This patent application is incorporated herein by reference.

Please replace paragraph [0019] with the following amended paragraph:

[0019] More detailed description of CRC generator 152 can be found in a copending patent application entitled "Network Physical Layer with Embedded Multi-Standard CRC Generator," filed concurrently on March 1, 2002 by Sasaki et al., Patent Application Serial Number 10/090,519. This patent application is incorporated herein by reference.

Please replace paragraph [0023] with the following amended paragraph:

[0023] The data in FIFO buffer 156 is delivered to serializer 158, which multiplexes parallel digital data to a serial bit stream for transmission over a serial link. The serial bit stream is sent to a transmit buffer 162 that drives the serial bit stream

onto a pair of differential serial output connections in output port 132. A configuration option of serializer 158 is to transmit 20 bits (high speed) or 10 bits (low speed) of data per reference clock cycle. More detailed description of this aspect of the invention can be found in a copending patent application entitled "Method And Apparatus For Operating A Transceiver In Different Data Rates," filed concurrently on March 1, 2002 by Cory, Patent Application Serial Number 10/090,251. This patent application is incorporated herein by reference.